Semiconductors

AN10038

Interfacing the ISP1582 to the Intel® PXA250 Processor

Rev. 02 — 2 March 2005 Application note

Document information

Info	Content
Keywords	isp1582, usb, universal serial bus, pxa250
Abstract	This document explains the interface between the ISP1582 and the Intel® Cotulla processor PXA250.

PHILIPS

Revision history

Rev	Date	Description
2.0	20050302	Second release. Updated Fig 1.
1.0	20040601	First release.

Contact information

For additional information, please visit: http://www.semiconductors.philips.com

For sales office addresses, please send an email to: sales.addresses@www.semiconductors.philips.com

1. Introduction

This document explains interfacing the ISP1582 to the Intel® Cotulla PXA250 processor.

2. Interfacing signals

The main ISP1582 signals to consider for connecting to an Intel Cotulla PXA250 processor are:

- A 16-bit data bus (DATA[15:0]) for the ISP1582.
- Eight address lines (A[7:0]) necessary for complete addressing of the ISP1582 internal registers.
- The CS_N line is used to select the ISP1582 in a certain address range of the host system. This input signal is active LOW.
- RD_N and WR_N are common read and write signals. These signals are active LOW.
- DMA channel standard control lines: DREQ, DACK, DIOR and DIOW.
- INT line: It is programmable type—level or edge, and polarity (active HIGH or LOW).
- The RESET_N signal is active LOW.

3. Interface block diagram

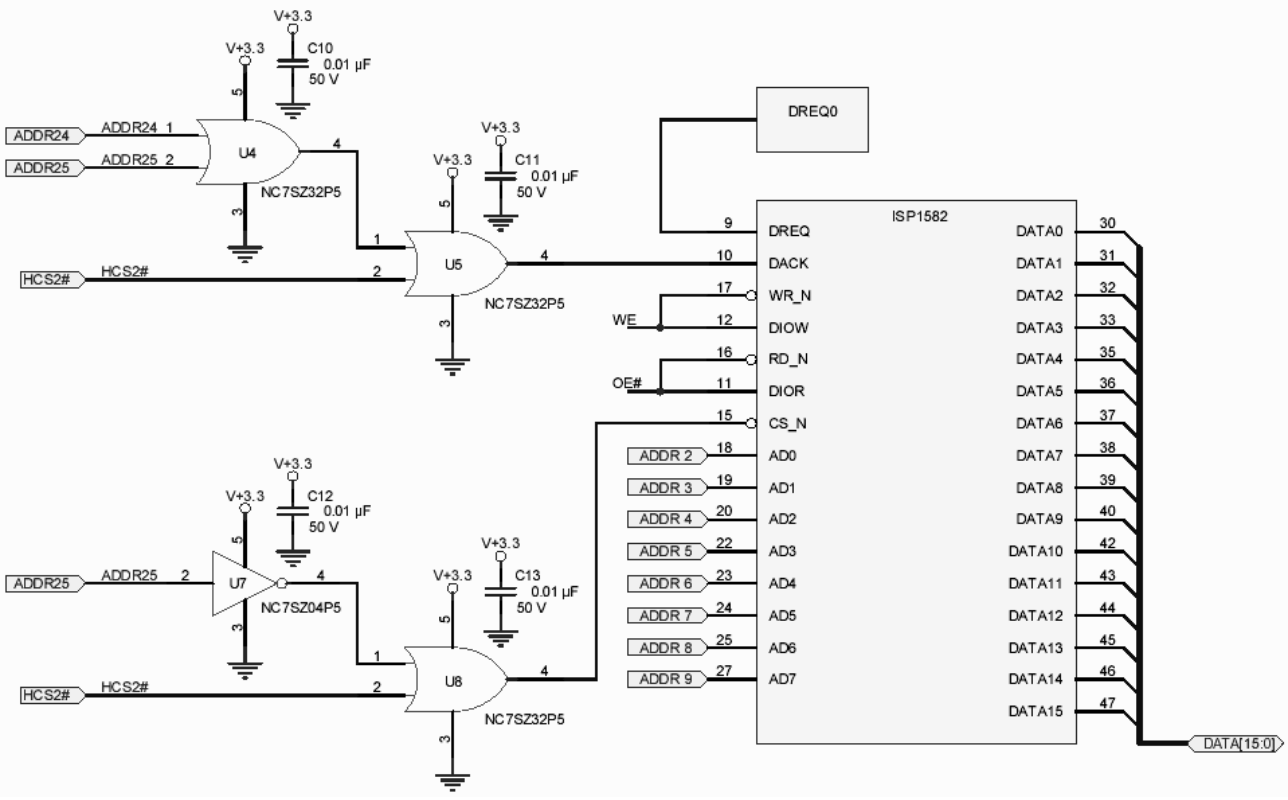

Fig 1. Interfacing block diagram.

For direct memory access (DMA) to the ISP1582 from the Cotulla chip, the following addresses are used. Using simple logic gates in between Cotulla and the ISP1582 can generate the required DACK signals.

Processor used: CS2#

PIO address map: 0000 0000h–00FF FFFFh

DMA channel 0 address map: 0200 0000h–02FF FFFFh

Remark: The DMA must be properly terminated before performing the PIO access if there is an interrupt during the DMA.

In Fig 1, it is assumed that the Parallel I/O (PIO) and the DMA use this memory spaces. You may choose a different configuration, depending on your requirement.

Fig 2 shows the PXA250 processor interface.

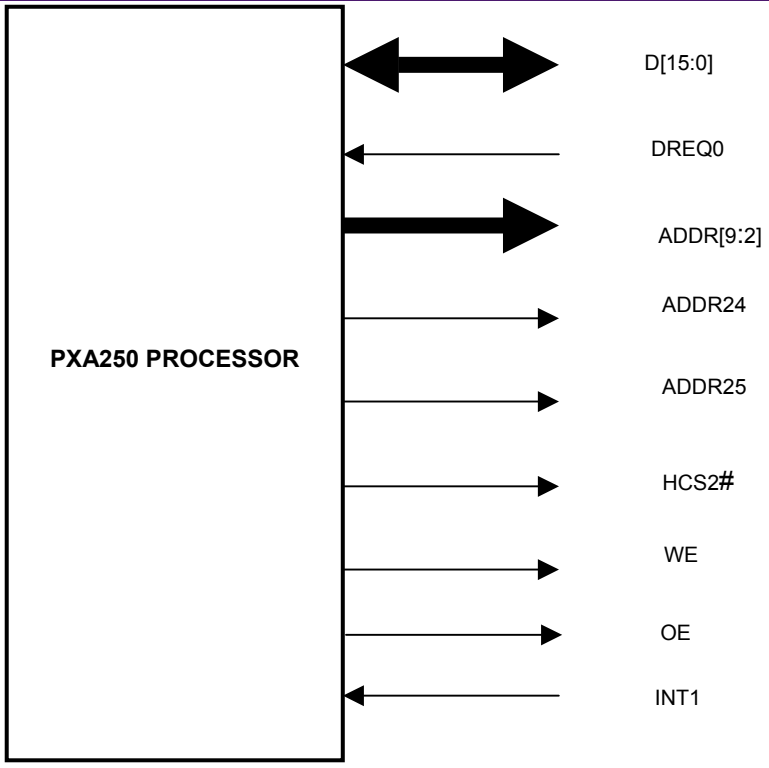

Fig 2. PXA250 processor.

4. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

5. Trademarks

Intel — is a registered trademark of Intel Corporation.

6. Contents

Date of release: 2 March 2005

Published in The Netherlands